A1 amended

wherein the memory device is controlled so that read data is read out successively when another of the plurality of word lines is activated.

Please add new claims 7 through 13 as follows:

A2

7. A memory device comprising:

a plurality of memory cells;

a plurality of sense amplifiers;

a plurality of read gates communicating with a read bus;

a plurality of write gates communicating with a write bus;

wherein each of the memory cells connects to the read bus through a read gate and a first sense amplifier that are positioned in series;

wherein each of the memory cells connects to the read bus through a read gate and a second sense amplifier that are positioned in series;

wherein each of the memory cells connects to the write bus through a write gate and the first sense amplifier that are positioned in series;

wherein each of the memory cells connects to the write bus through a write gate and the second sense amplifier that are positioned in series; and

wherein the first sense amplifier and the second sense amplifier are positioned in parallel, whereby data is able to be transferred through both parallel sense amplifiers during read and write operations.

8. The memory device according to Claim 7, wherein the read gate in series with the first sense amplifier is a same read gate as the read gate positioned in series with the second sense amplifier.

9. The memory device according to Claim 7, wherein the write gate in series with the first sense amplifier is a same write gate as the write gate positioned in series with the second sense amplifier.

10. The memory device according to Claim 7, wherein the read gate in series with the first sense amplifier is a different read gate from the read gate positioned in series with the second sense amplifier.

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